SHF-0289 Amplifier Application Circuits

Abstract

Sirenza Microdevices' SHF-0289 is a high performance AlGaAs/GaAs Heterostructure FET (HFET) housed in a low-cost surface-mount plastic package. The HFET technology improves breakdown voltage while minimizing Schottky leakage current, resulting in higher power added efficiency and improved linearity. This application note illustrates several application circuits for key frequency bands in the 800-2200 MHz spectrum.

Introduction

The application circuits were designed to achieve the optimum combination of P1dB, OIP3, and (W)CDMA channel power. These designs illustrate the general performance capabilities of the device under true class AB operation. Users may wish to modify these designs to achieve optimum performance under specific input conditions and system requirements. All recommended components are standard values available from well-known manufacturers. Components specified in the bill of materials (BOM) have known parasitics which in some cases are critical to the circuit's performance. Deviating from the recommended BOM may result in a performance shift due to varying parasitics. Matching component placement is critical to each circuit's performance.

Circuit Details

SMDI will provide the detailed layout (AutoCad format) to users wishing to use the exact same layout and substrate material shown in the following circuits. The circuits recommended within this application note were designed using the following PCB material:

Material: GETEK™ ML200C
Core thickness: 0.031"
Copper cladding: 2 oz. finish
Dielectric constant: 4.1
Dielectric loss tangent: 0.0089 (@ 1 GHz)

Customers not wishing to use the exact material and layouts shown in this application note can design their own PCB using the critical transmission line impedances and phase lengths shown in the BOMs and layouts.

Design Considerations and Trade-offs

1. The SHF-0289 is a depletion mode FET and requires a negative gate-to-source voltage. Normal pinchoff variation from part-to-part generally precludes the use of the same fixed gate voltage for all devices. Active bias circuitry or manual gate bias alignment is recommended to maintain acceptable performance (RF and thermal).

2. For large signal operation class AB biasing is required to maximize the FET's performance. Passive gate bias circuitry is generally required to achieve pure class AB performance. Per item 1 above, the gate voltage should be aligned for each device to eliminate the effects of pinchoff variation.

3. Active bias circuitry is strongly recommended for small signal, class A operation. The use of active bias circuitry will eliminate the effects of pinchoff variation without compromising the power and linearity performance of the FET under small signal conditions. Be sure to consider the impact of large peak-to-average ratios with less than 10dB backoff.

4. Choose the operating voltage based on the amount of backoff. General guidelines are as follows: For large signal operation, the drain-source voltage should be increased to 8V to maximize P1dB. For small signal operation, the OIP3 can be maximized by reducing the voltage to 6-7 V and increasing the current. The application circuits that follow should be re-optimized if the recommended baseline bias condition is not used. Make sure the quiescent bias condition does not exceed the recommended power dissipation limit shown on page 1 of the datasheet.

Biasing Depletion Mode FETs

The SHF devices are depletion mode HFETs. As such, a negative gate-to-source (V_{GS}) voltage is required to control the drain current. A power supply sequencing circuit should be used to guarantee that the negative gate voltage is present before the drain voltage is applied. Simply put, the gate voltage should be "first on, last off". Without power supply sequencing circuitry, the FET may experience damaging voltage or current transients during turn-on.

Passive Biasing

Peak RF performance can generally only be achieved with passive bias circuitry. Class AB operation is generally required for large signal applications and complex modulation schemes with high peak-to-average ratios. Most active bias circuits limit the amplifer to class A operation.

The conventional passive bias circuit is a voltage divider from a fixed negative supply (-3 to -5V). Because gate current increases with RF drive level, the series gate resistance should be kept small to minimize its pinchoff effect during large signal operation. Temperature compensation circuitry can be added to the voltage divider network to maintain constant quiescent current over temperature. The linearity of the device is a strong function of quiescent current.

Due to the normal pinchoff variation inherent to HFETs, an adjustable voltage divider is recommended, when a passive bias is used. This is most commonly accomplished with a potentiometer in one section of the voltage divider. The potentiometer then allows for the quiescent current to be aligned for each device.

Biasing with a fixed V_{GS} is not recommended, and may result in inconsistent drain current from part-to-part. In extreme cases, the RF performance or power dissipation may no longer meet the designer's specifications and/or the device's max ratings. For fixed-divider designs, the quiescent current should be measured on each device to ensure that it remains in an acceptable range.

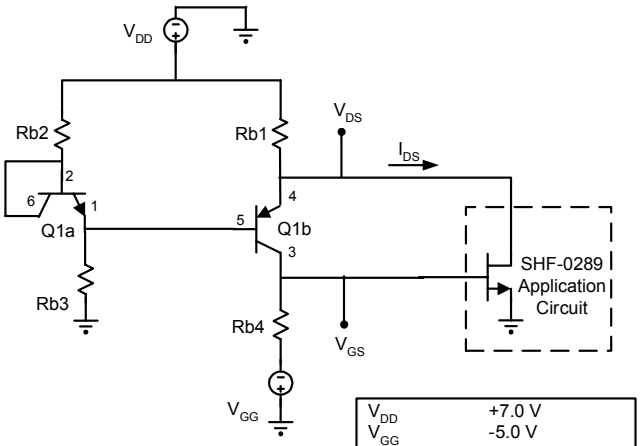
If a fixed resistor divider is used, the amount of gate voltage alignment required can be minimized by presetting the voltage divider on a lot-by-lot basis. By measuring a small sample of parts, the average gate voltage can quickly be determined for each SHF lot. This technique will not entirely eliminate the need for post-assembly bias adjustment. It will however prevent large errors from lot-to-lot.

Active Biasing

For small signal and/or class A operation, SMDI recommends the use of an active bias circuit to eliminate the effects of pinchoff variation. The designer should choose an active bias circuit that best meets his system's cost, complexity, and performance requirements. The bias circuit shown below not only negates the effects of pinchoff variation, but also provides excellent temperature compensation from –40C to +85C. The circuit requires a modest 0.2-0.4V drop from the positive supply rail to effectively regulate the drain current over temperature. The circuit below is configured to operate from –5V and +7V DC supplies.

The circuit may be operated from other voltages by simply changing the resistors in the bias circuit. A spreadsheet design tool is available for this active bias circuit. The spreadsheet can be accessed from the SHF-0289 homepage on our website at www.sirenza.com. Contact our Discrete Applications Support Team via email at disc-apps@sirenza.com if you need help modifying this bias circuit. Differential op-amps are also commonly used to control the gate voltage and maintain a constant drain current.

As with most active bias schemes, the circuit below primarily limits the amplifier to class A operation. Some drive-up may occur but true class AB operation is not typical. Note that the application circuit results herein were not measured using an active bias circuit. Rather, the circuits were biased directly from two power supplies such to demonstrate the full capability of the amplifier under true class AB operation. Similar performance can be achieved with passive bias circuits. (see 'Passive Biasing' section).



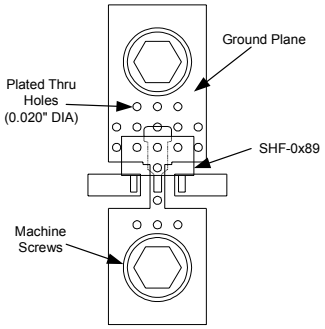
SHF-0289 Active Bias Circuit

V_{DD}	+7.0 V
V_{GG}	-5.0 V
I_{DS}	200 mA
Rb1	1.5 ohms
Rb2	300 ohms
Rb3	6.1K ohms
Rb4	3.9K ohms
Q1	UMZ1N (ROHM)

Mounting and Thermal Considerations

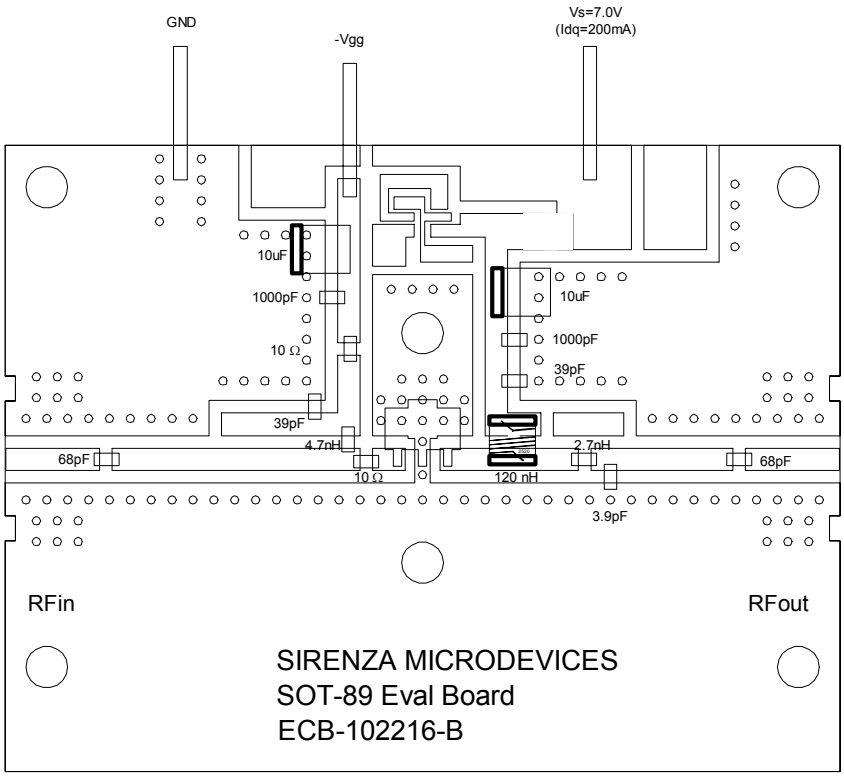
It is very important that adequate heat sinking be provided to minimize the device junction temperature. The following items should be implemented to maximize MTTF and RF performance.

1. Multiple solder-filled vias are required directly below the ground tab (pin 4). [CRITICAL]
2. Incorporate a large ground pad area with multiple plated-through vias around pin 4 of the device. [CRITICAL]
3. Use two point board seating to lower the thermal resistance between the PCB and mounting plate. Place machine screws as close to the ground tab (pin 4) as possible. [CRITICAL]
4. Use 2 ounce copper to improve the PCB's heat spreading capability. [CRITICAL]
5. Thermal transfer paste should be used between the PCB and the mounting plate to improve heat spreading capability. [RECOMMENDED]



Recommended Mounting Configuration

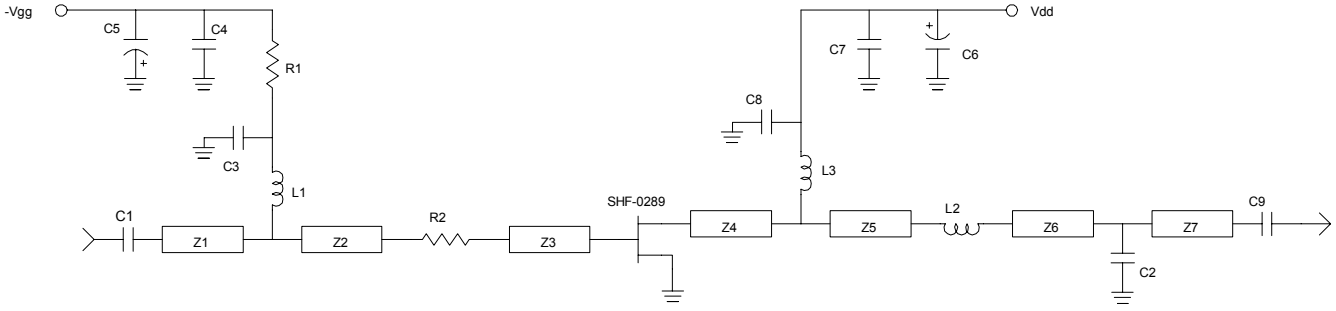
870-960 MHz Application Circuit (V_{DS}=7V, I_{DQ}=200mA, 25°C)



Ref. desig.	Value	Part Number /Style
C1,9	68 pF	ROHM MCH185A680JK
C3,8	39 pF	ROHM MCH185A390JK
C4,7	1000 pF	ROHM MCH185CN102KK
C5,6	10 uF	KOA TMC1DB106KLRH
C2	3.9 pF	ROHM MCH185A3R9CK
L1	4.7 nH	TOKO LL1608-FS4N7S
L2	2.7 nH	TOKO LL1608-FS2N7S
L3	120 nH	Coilcraft 1008CS-121X-BC
R1,2	10 ohms	ROHM MCR03J100

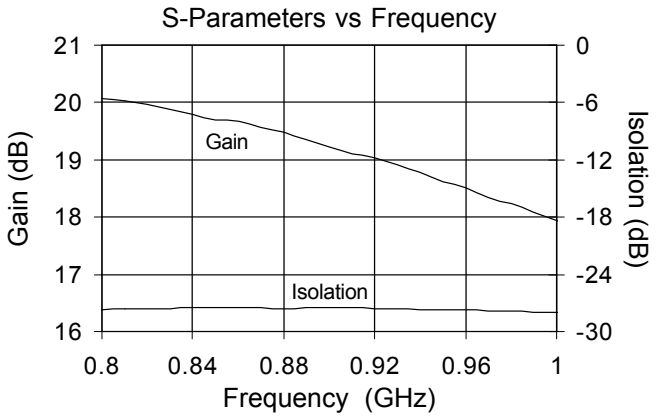
Microstrip Segment Specifications:

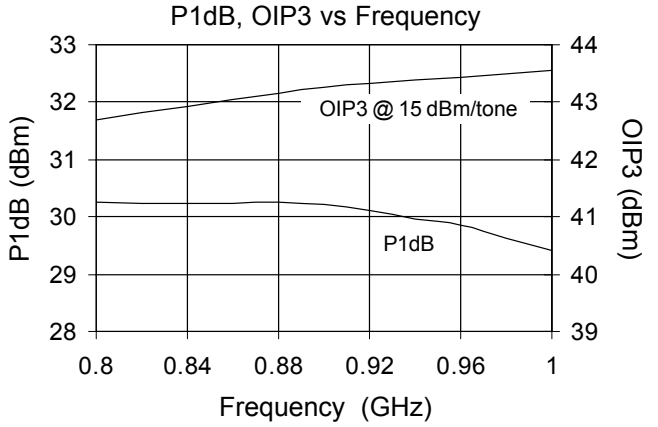
Ref. desig.	Value
Z1	50 ohms, non-critical
Z2	50 ohms, 1.3 deg. @ 900 MHz
Z3	50 ohms, 3.6 deg. @ 900 MHz
Z4	50 ohms, 8.0 deg. @ 900 MHz
Z5	50 ohms, 7.3 deg. @ 900 MHz
Z6	50 ohms, 2.2 deg. @ 900 MHz
Z7	50 ohms, non-critical

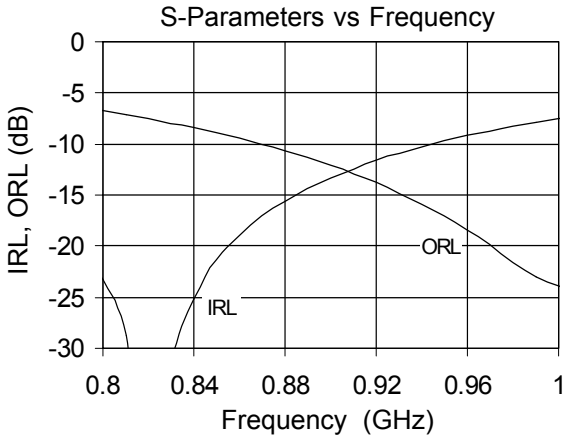


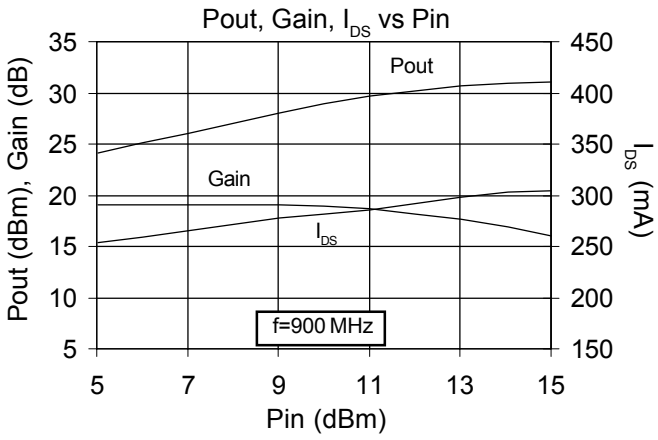
SHF-0289 915 MHz Application Circuit

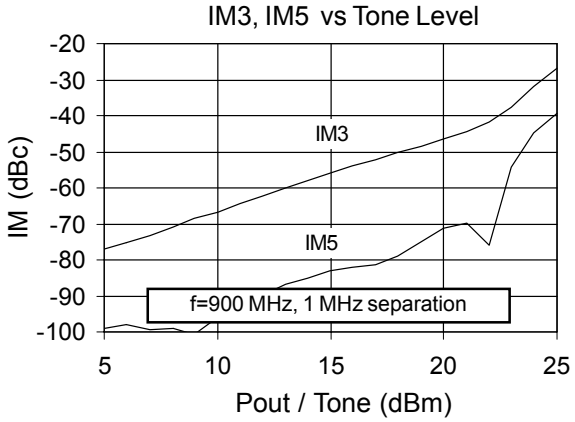
Typical Performance - 870-960 MHz Application Circuit (V_{DS}=7V, I_{DQ}=200mA, 25°C)

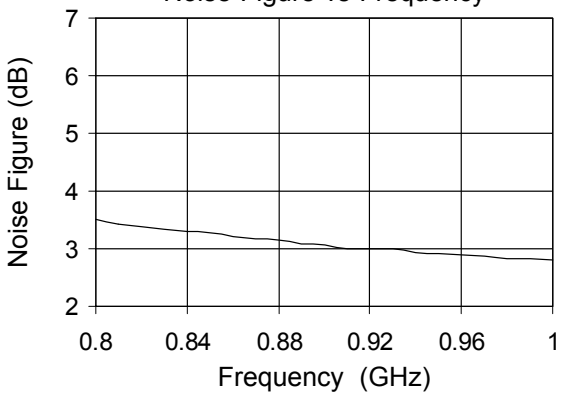






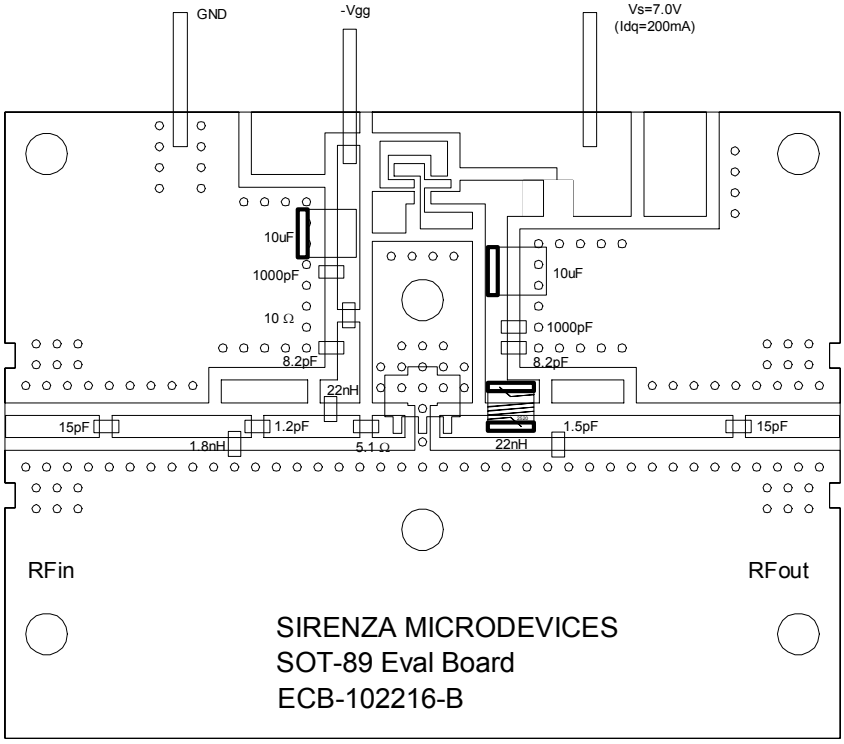






Freq (GHz)	P1dB (dBm)	OIP3 (dBm)	Gain (dB)	S11 (dB)	S22 (dB)	NF (dB)
0.880	30.3	42.6	19.4	-16	-10	3.1
0.915	30.2	43.2	19.2	-12	-14	3.0
0.945	30.0	42.7	18.6	-10	-16	2.9

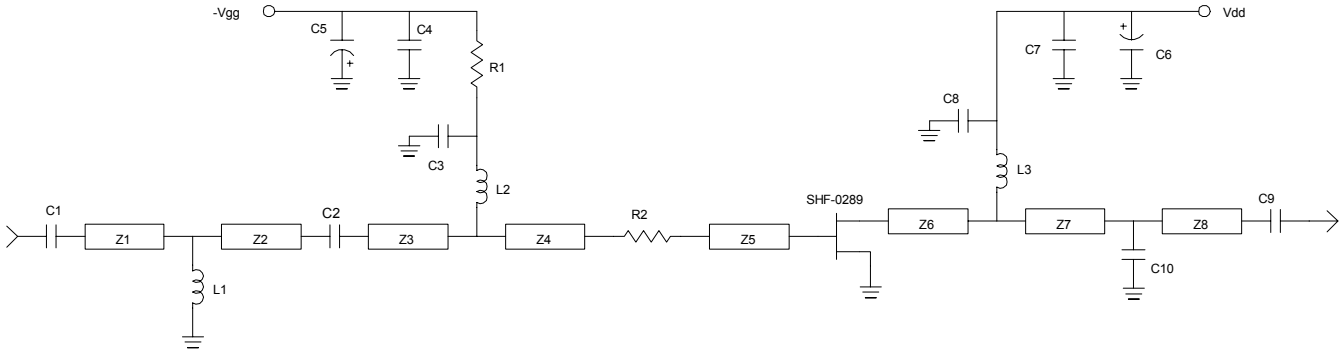
1930-1990 MHz Application Circuit (V_{DS}=7V, I_{DQ}=200mA, 25°C)



Ref. desig.	Value	Part Number /Style
C1,9	15 pF	ROHM MCH185A150J
C2	1.2 pF	ROHM MCH185A1R2C
C3,8	8.2 pF	ROHM MCH185A8R2D
C5,6	10 uF	KOA TMC1DB106KLRH
C4,7	1000 pF	ROHM MCH185CN102K
C10	1.5 pF	ROHM MCH185A1R5C
L1	1.8 nH	TOKO LL1608-FS1N8S
L2	22 nH	TOKO LL1608-FS22NJ
L3	22 nH	Coilcraft 1008CS-220X-BC
R1	10 ohms	ROHM MCR03J100
R2	5.1 ohms	ROHM MCR03J5R1

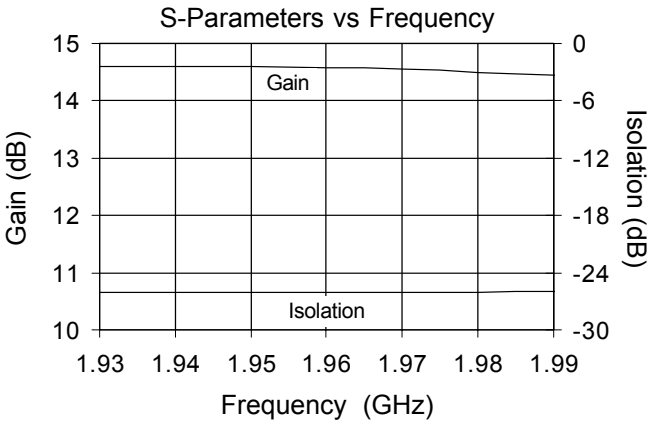
Microstrip Segment Specifications:

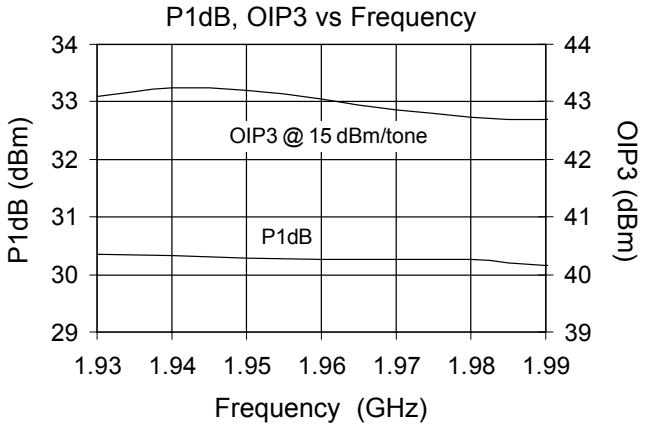
Ref. desig.	Value
Z1	50 ohms, non-critical
Z2	50 ohms, 4.0 deg. @ 1960 MHz
Z3	50 ohms, 16.2 deg. @ 1960 MHz
Z4	50 ohms, 7.1 deg. @ 1960 MHz
Z5	50 ohms, 7.9 deg. @ 1960 MHz
Z6	50 ohms, 17.1 deg. @ 1960 MHz
Z7	50 ohms, 11.5 deg. @ 1960 MHz
Z8	50 ohms, non-critical

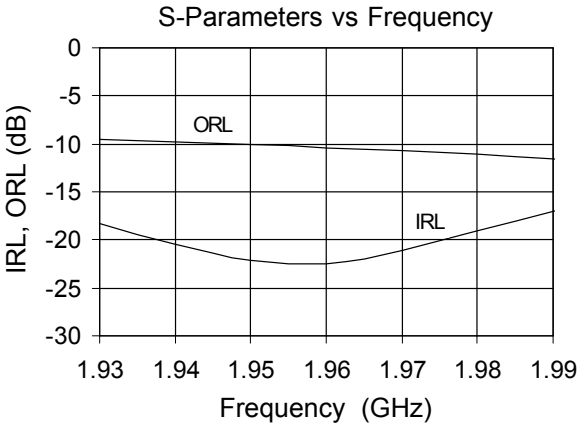


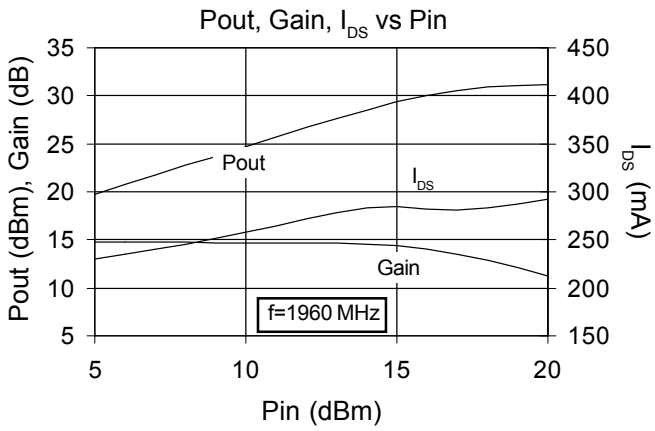
SHF-0289 1960 MHz Application Circuit

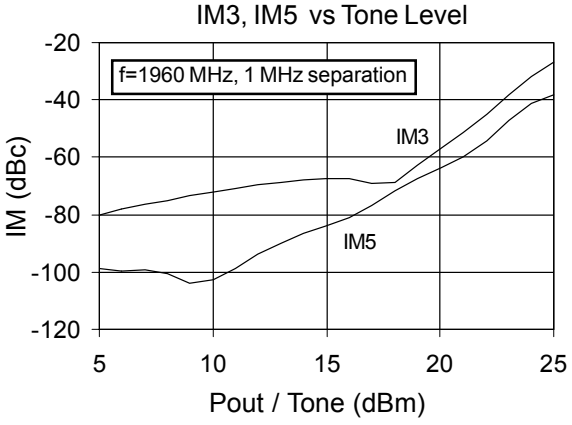
Typical Performance - 1930-1990 MHz Application Circuit (V_{DS}=7V, I_{DQ}=200mA, 25°C)

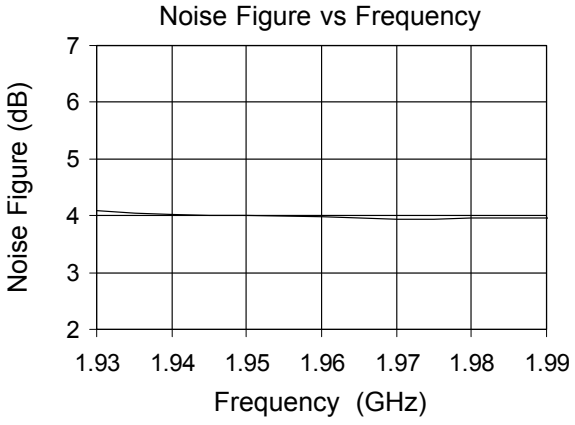






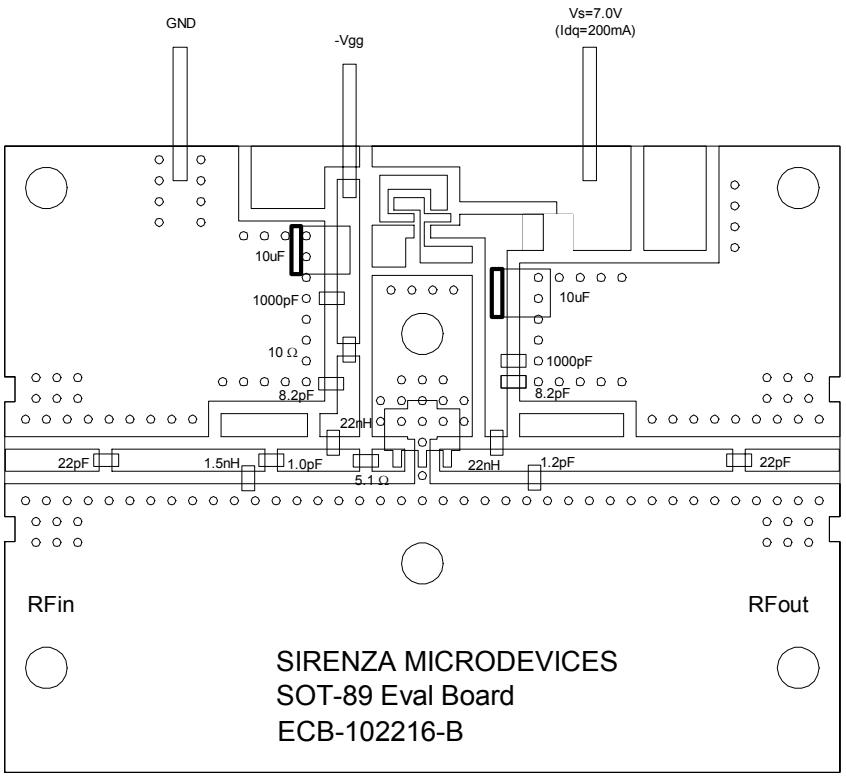






Freq (GHz)	P1dB (dBm)	OIP3 (dBm)	Gain (dB)	S11 (dB)	S22 (dB)	NF (dB)
1.93	30.3	43.1	14.6	-18	-9	4.1
1.96	30.3	43.1	14.6	-22	-10	4.0
1.99	30.2	42.7	14.4	-17	-11	4.0

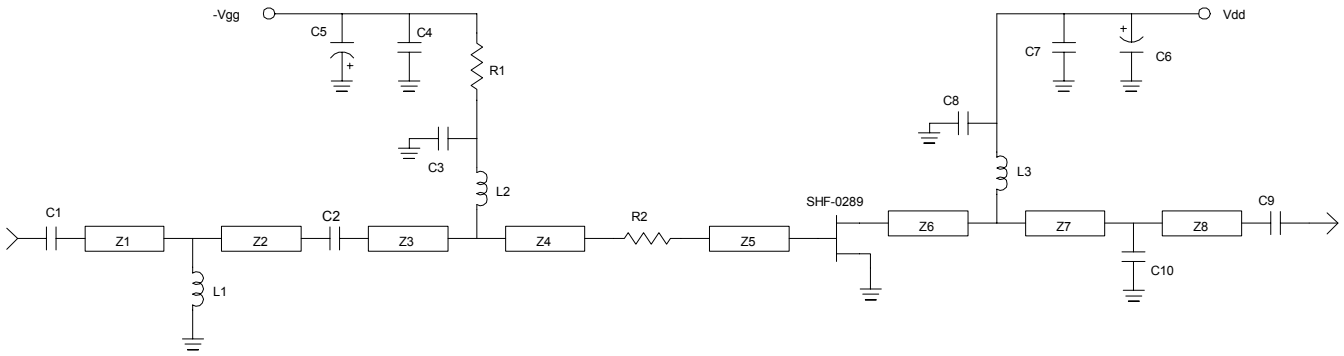
2140 MHz Application Circuit (V_{DS}=7V, I_{DQ}=200mA, 25°C)



Ref. desig.	Value	Part Number /Style
C1,9	22 pF	ROHM MCH185A220JK
C3,8	8.2 pF	ROHM MCH185A8R2DK
C4,7	1000 pF	ROHM MCH185CN102KK
C5,6	10 uF	KOA TMC1DB106KLRH
C2	1.0 pF	ROHM MCH185A010CK
C10	1.2 pF	ROHM MCH185A1R2CK
L1	1.5 nH	TOKO LL1608-FS1N5S
L2,3	22 nH	TOKO LL1608-FS22NJ
R1	10 ohms	ROHM MCR03J100
R2	5.1 ohms	ROHM MCR03J5R1

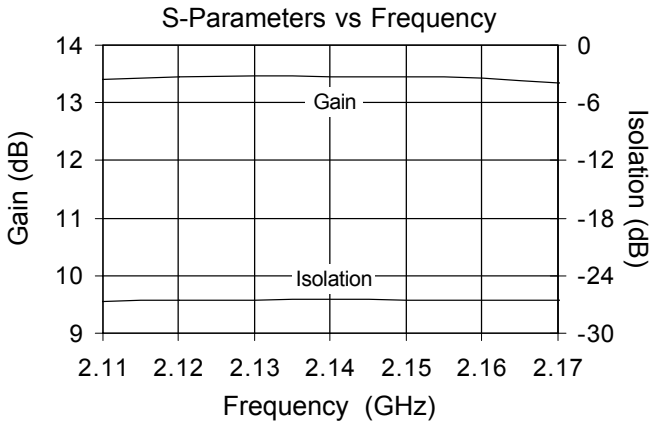
Microstrip Segment Specifications:

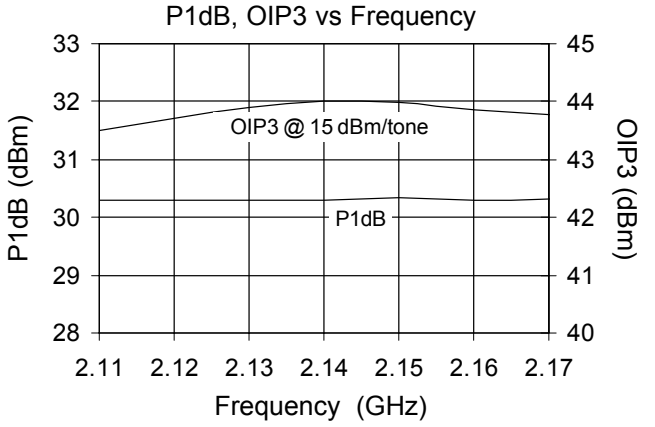
Ref. desig.	Value
Z1	50 ohms, non-critical
Z2	50 ohms, 4.6 deg. @ 2140 MHz
Z3	50 ohms, 14.7 deg. @ 2140 MHz
Z4	50 ohms, 6.9 deg. @ 2140 MHz
Z5	50 ohms, 8.6 deg. @ 2140 MHz
Z6	50 ohms, 15.1 deg. @ 2140 MHz
Z7	50 ohms, 9.9 deg. @ 2140 MHz
Z8	50 ohms, non-critical

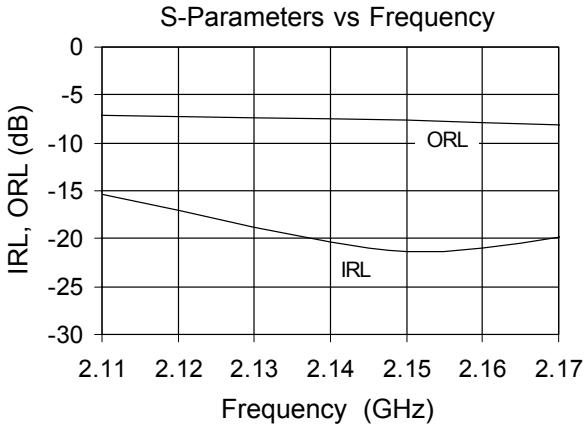


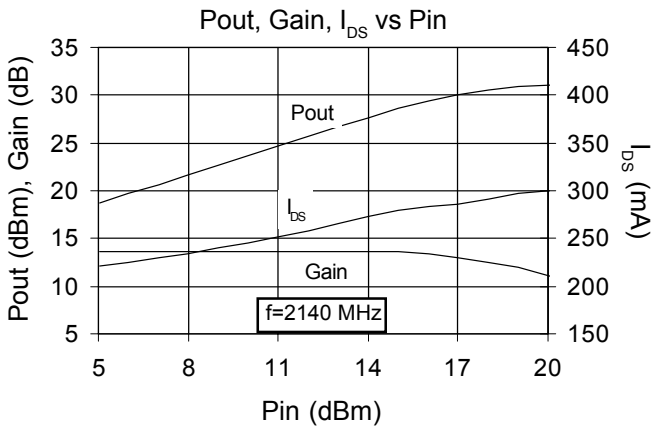
SHF-0289 2140 MHz Application Circuit

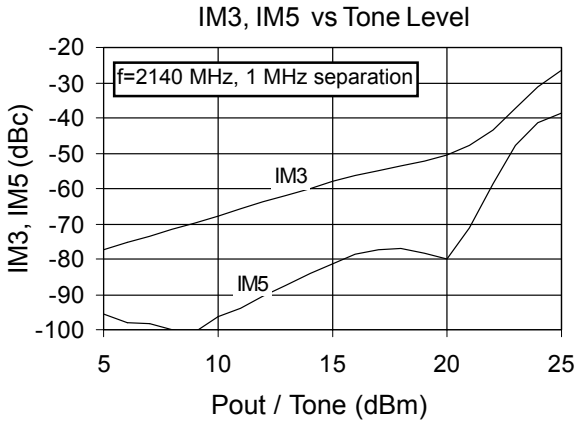
Typical Performance - 2140 MHz Application Circuit (V_{DS}=7V, I_{DQ}=200mA, 25°C)

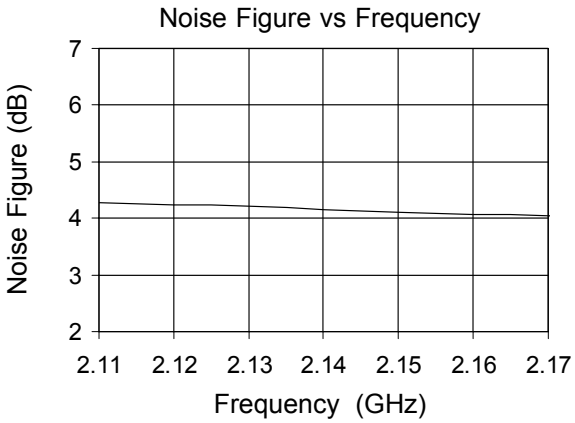












Freq (GHz)	P1dB (dBm)	OIP3 (dBm)	Gain (dB)	S11 (dB)	S22 (dB)	NF (dB)
2.11	30.3	43.5	13.4	-15	-8	4.3
2.14	30.3	44.0	13.4	-20	-8	4.2
2.17	30.3	43.7	13.4	-19	-8	4.0